

CLAIMS

We claim:

1        1. A delay element comprising:

2            an amplifier adapted to receive input signals;

3            a filter coupled to the amplifier and adapted to provide a  
4 variable delay, wherein the filter comprises:

5            a first inductor having a first terminal and a second  
6 terminal, the first terminal coupled to a first output terminal  
7 of the amplifier and the second terminal providing a first  
8 output signal of the delay element;

9            a second inductor having a third terminal and a fourth  
10 terminal, the third terminal coupled to a second output terminal  
11 of the amplifier and the fourth terminal providing a second  
12 output signal of the delay element;

13            at least a first capacitor coupled between the first  
14 output terminal of the amplifier and the fourth terminal of the  
15 second inductor, wherein a capacitance of the at least first  
16 capacitor is variable; and

17            at least a second capacitor coupled between the second  
18 output terminal of the amplifier and the second terminal of the  
19 first inductor, wherein a capacitance of the at least second  
20 capacitor is variable.

1       2. The delay element of Claim 1, wherein the filter  
2 further comprises:

3       at least a third capacitor coupled between the fourth  
4 terminal of the second inductor and a reference terminal,  
5 wherein a capacitance of the at least third capacitor is  
6 variable; and

7       at least a fourth capacitor coupled between the second  
8 terminal of the first inductor and the reference terminal,  
9 wherein a capacitance of the at least fourth capacitor is  
10 variable.

1       3. The delay element of Claim 2, wherein the reference  
2 terminal is at a ground voltage potential.

1       4. The delay element of Claim 2, wherein the amplifier is  
2 a differential amplifier comprising:

3       a pair of transistors;

4       a pair of resistors coupled between a supply voltage and  
5 corresponding ones of the transistors; and

6       a current source coupled between the pair of transistors  
7 and the reference terminal.

1       5. The delay element of Claim 2, wherein the at least  
2 first and second capacitors each comprises:  
  
3           a first fixed capacitor;  
  
4           at least one selectable fifth capacitor coupled in parallel  
5 with the first fixed capacitor; and  
  
6           a first transistor in series with each selectable fifth  
7 capacitor and adapted to be controlled to determine whether the  
8 associated selectable fifth capacitor is enabled.

1       6. The delay element of Claim 5, wherein the at least  
2 third and fourth capacitors each comprises:  
  
3           a second fixed capacitor;  
  
4           at least one selectable sixth capacitor coupled in parallel  
5 with the second fixed capacitor; and  
  
6           a second transistor in series with each selectable sixth  
7 capacitor and adapted to be controlled to determine whether the  
8 associated selectable sixth capacitor is enabled.

1       7. The delay element of Claim 2, wherein the delay  
2 element is programmable for the variable delay and to account  
3 for semiconductor processing variations.

1       8. The delay element of Claim 2, wherein the filter is an  
2 allpass filter and the delay element is adapted to provide an  
3 approximately flat magnitude and group delay response across a  
4 frequency range.

1        9. The delay element of Claim 1, wherein the amplifier is  
2 a differential amplifier.

1        10. An equalizer comprising:

2            a feedforward filter adapted to receive a first input  
3 signal and provide a first output signal, wherein the  
4 feedforward filter comprises at least one delay element having a  
5 variable delay;

6            an adaptive coefficient generator adapted to receive the  
7 first input signal and a second signal and provide tap  
8 coefficients to the feedforward filter;

9            a slicer adapted to receive a slicer input signal and  
10 provide a slicer output signal;

11          a slicer timing alignment block adapted to receive the  
12 slicer input signal and provide a second output signal, wherein  
13 the slicer output signal is subtracted from the second output  
14 signal to generate an error signal;

15          a tap timing alignment block adapted to receive the slicer  
16 output signal and provide a third output signal; and

17          a first low pass filter adapted to receive the third output  
18 signal and the error signal and provide a fourth output signal,  
19 wherein the fourth output signal is multiplied with the third  
20 output signal to provide a feedback signal which is added to the  
21 first output signal to generate the slicer input signal.

1        11. The equalizer of Claim 10, wherein the delay element  
2 comprises:

3            a first inductor having a first terminal and a second  
4 terminal, the first terminal adapted to receive a first delay  
5 element signal and the second terminal providing a first delay  
6 element output signal of the delay element;

7            a second inductor having a third terminal and a fourth  
8 terminal, the third terminal adapted to receive a second delay  
9 element signal and the fourth terminal providing a second delay  
10 element output signal of the delay element;

11           a first capacitor coupled between the first terminal of the  
12 first inductor and the fourth terminal of the second inductor,  
13 wherein a capacitance of the first capacitor is variable; and

14           a second capacitor coupled between the third terminal of  
15 the second inductor and the second terminal of the first  
16 inductor, wherein a capacitance of the second capacitor is  
17 variable.

1        12. The equalizer of Claim 11, wherein the delay element  
2 further comprises an amplifier adapted to receive input signals  
3 and provide the first delay element signal to the first inductor  
4 and the second delay element signal to the second inductor.

1        13. The equalizer of Claim 12, wherein the delay element  
2 further comprises:

3            a third capacitor coupled between the fourth terminal of  
4 the second inductor and a reference terminal, wherein a  
5 capacitance of the third capacitor is variable; and

6            a fourth capacitor coupled between the second terminal of  
7 the first inductor and the reference terminal, wherein a  
8 capacitance of the fourth capacitor is variable.

1        14. The equalizer of Claim 13, wherein the first and  
2 second capacitors each comprises:

3            a first fixed capacitor;

4            at least one selectable fifth capacitor coupled in parallel  
5 with the first fixed capacitor; and

6            a first transistor in series with each selectable fifth  
7 capacitor and adapted to be controlled to determine whether the  
8 associated selectable fifth capacitor is enabled.

1        15. The equalizer of Claim 14, wherein the third and  
2 fourth capacitors each comprises:

3            a second fixed capacitor;

4            at least one selectable sixth capacitor coupled in parallel  
5 with the second fixed capacitor; and

6            a second transistor in series with each selectable sixth  
7 capacitor and adapted to be controlled to determine whether the  
8 associated selectable sixth capacitor is enabled.

1        16. The equalizer of Claim 10, wherein the adaptive  
2 coefficient generator and/or the slicer timing alignment block  
3 comprises at least one delay element having a variable delay.

1        17. The equalizer of Claim 10, wherein the delay element  
2 comprises:

3            an amplifier adapted to receive input signals and provide a  
4 first delay element signal and a second delay element signal;

5            a first and a second inductor in series, wherein the first  
6 inductor receives the first delay element signal at a first  
7 terminal and the second inductor provides a first delay element  
8 output signal at a second terminal;

9            a first capacitor coupled between the first and second  
10 inductor and a reference terminal;

11          a third and a fourth inductor in series, wherein the third  
12 inductor receives the second delay element signal at a third  
13 terminal and the fourth inductor provides a second delay element  
14 output signal at a fourth terminal;

15          a second capacitor coupled between the third and fourth  
16 inductor and the reference terminal;

17          a third capacitor coupled to the first terminal and the  
18 fourth terminal;

19          a fourth capacitor coupled to the third terminal and the  
20 second terminal;

21          a fifth capacitor coupled to the second terminal and the  
22 reference terminal; and

23        a sixth capacitor coupled to the fourth terminal and the  
24    reference terminal.

1        18. The equalizer of Claim 17, wherein the third, fourth,  
2    fifth, and sixth capacitor are adapted to have a variable  
3    capacitance.

1        19. A method of providing a variable signal delay, the  
2    method comprising:

3        receiving an input signal;

4        amplifying the input signal to provide an amplified output  
5    signal;

6        passing the amplified output signal through a filter having  
7    inductors and cross-coupled capacitors whose capacitance is  
8    variable; and

9        providing an output signal across load capacitors of the  
10   filter whose capacitance is variable to provide a desired signal  
11   delay.

1        20. The method of Claim 19, wherein the capacitance of the  
2    cross-coupled capacitors is variable to account for  
3    semiconductor processing variations.

1        21. The method of Claim 19, wherein the filter is an  
2    allpass filter adapted to provide an approximately constant  
3    group delay and magnitude response over a frequency range.

1        22. A method of providing a signal delay, the method  
2 comprising:

3        providing an amplifier adapted to amplify input signals and  
4 provide amplified output signals; and

5        providing a filter adapted to filter the amplified output  
6 signals, the filter having cross-coupled capacitors and load  
7 capacitors whose capacitance is variable to provide a selectable  
8 signal delay.

1        23. The method of Claim 22, wherein the capacitance of the  
2 cross-coupled capacitors is variable to account for  
3 semiconductor processing variations.

1        24. The method of Claim 22, wherein the filter is an  
2 allpass filter adapted to provide an approximately flat  
3 magnitude and group delay response across a frequency range.

1        25. A delay element comprising:

2            an amplifier adapted to receive input signals and provide a  
3        first signal and a second signal;

4            a first and a second inductor in series, wherein the first  
5        inductor receives the first signal at a first terminal and the  
6        second inductor provides a first output signal at a second  
7        terminal;

8            a first capacitor coupled between the first and second  
9        inductor and a reference terminal;

10          a third and a fourth inductor in series, wherein the third  
11       inductor receives the second signal at a third terminal and the  
12       fourth inductor provides a second output signal at a fourth  
13       terminal;

14          a second capacitor coupled between the third and fourth  
15       inductor and the reference terminal;

16          a third capacitor coupled to the first terminal and the  
17       fourth terminal;

18          a fourth capacitor coupled to the third terminal and the  
19       second terminal;

20          a fifth capacitor coupled to the second terminal and the  
21       reference terminal; and

22          a sixth capacitor coupled to the fourth terminal and the  
23       reference terminal.

1        26. The delay element of Claim 25, wherein the third,  
2       fourth, fifth, and sixth capacitor are adapted to have a  
3       variable capacitance.

1        27. The delay element of Claim 25, wherein the third,  
2        fourth, fifth, and sixth capacitor each comprises a fixed  
3        capacitor in parallel with a selectively enabled capacitor.